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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,758	12/30/2003	Warren R. Morrow	42P17981	2703
<div>7590      08/23/2007</div> <div>Jan Little-Washington BLAKELY, SOKOLOFF, TAYLOR &amp; ZAFMAN LLP Seventh Floor 12400 Wilshire Boulevard Los Angeles, CA 90025</div>				
			<div>EXAMINER</div> <div>LIN, PHYOWAI</div>	
			<div>ART UNIT</div> <div>2613</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE</div> <div>08/23/2007</div>	<div>DELIVERY MODE</div> <div>PAPER</div>

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/748,758

Applicant(s)

MORROW ET AL.

Examiner

PHYOWAI LIN

Art Unit

2613

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 December 2003 and 18 October 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 07/06/2005.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

2. The references listed in the Information Disclosure Statement filed on July 6, 2005 have been considered by the examiner (see attached PTO-1449 form).

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-21** are rejected under 35 U.S.C. 102(e) as being anticipated by Levy et al. (US Pub Number 2004/0126115).

**Regarding claim 1**, Levy et al. disclose an apparatus (see FIG.5), comprising:

an integrated circuit (a substrate) to communicate with a memory (memory device 12), the integrated circuit having an optical transmitter (OT&R) (see paragraph [0020], lines 8-11; paragraph [0020], lines 2-4 and FIG.5) ;

an optical bus (optical connection system 51) coupled to the optical transmitter (see paragraph [0020], lines 4-6 and FIG.5);

Art Unit: 2613

N optical receivers (receiver 61) coupled to the optical bus via N optical couplers (light pipe or lenses 54) (see paragraph [0022], lines 1-8; FIG.5 and FIG.6a where in plurality of optical receivers inside the optical connector housings 33 couple to the optical bus through plurality of optical light pipe or lenses inside the optical connector housings 33);

N memory modules (DIMMs 30) coupled to the N optical receivers (see paragraph [0022], lines 17-19; FIG.5 and FIG.6a where in plurality of DIMM 31 couple to the plurality of optical receivers inside the optical connector housings 33); and

one or more memory devices (memory device 12) coupled to the N memory modules (DIMMs 30) (see paragraph [0020], lines 13-16 and FIG.5),

the optical transmitter to convert a signal to communicate with the memory devices from a first electrical signal (an electrical link 46) to an optical signal (see paragraph [0020], lines 2-4; paragraph [0035], lines 2-6 and FIG.5 where in the OT&R converts the electrical signal from the electrical link 46 to optical signal link 52 for communicating with DIMMs 30 which has memory device 12), the optical bus to propagate the optical signal (see paragraph [0020], lines 4-6 and FIG.5 where in optical bus 52 for propagating the optical signal in it), each of the N optical couplers to couple one-Nth of the optical signal from the optical bus to its associated optical receiver (see paragraph [0035], lines 1-5; FIG.6a and FIG.8 where in one-Nth of the optical signal from the optical bus 82 is coupled into one of the DIMMs 30 which includes optical receiver 61),

each optical receiver to convert its one-Nth of the optical signal to second set of electrical signals, the N memory modules to couple the second set of electrical signals to the memory devices (see paragraph [0018], lines 19-23 and FIG.3, FIG.6a and FIG.8 where in optical receiver 61 converting the optical signal to the second electrical signal using signal converter 35 which is on the substrate 31 inside the DIMMs 30 for usage by the memory device 12).

**Regarding to claim 2**, Levy et al. disclose everything claimed as applied above (see claim 1). In addition, Levy et al. disclose the apparatus further includes: wherein the integrated circuit is a memory controller (see paragraph [0018], lines 19-23 and FIG.5).

**Regarding to claim 3**, Levy et al. disclose everything claimed as applied above (see claim 1). In addition, Levy et al. disclose the apparatus further includes: wherein the integrated circuit is a processor (see FIG.8 where in the integrated circuit of memory controller and OT&R also couple with microprocessor).

**Regarding to claim 4**, Levy et al. disclose everything claimed as applied above (see claim 1). In addition, Levy et al. disclose the apparatus further includes: wherein the optical bus includes optical fiber (see paragraph [0028], lines 1-2 and FIG.5).

**Regarding to claim 5**, Levy et al. disclose everything claimed as applied above (see claim 1). In addition, Levy et al. disclose the apparatus further includes: wherein

the optical transmitter includes a laser (see FIG.5 where in it is well known in the art that a laser inherently exists in the optical transmitter (OT&R) for transmitting the optical light output).

**Regarding to claim 6**, Levy et al. disclose everything claimed as applied above (see claim 1). In addition, Levy et al. disclose the apparatus further includes: wherein the couplers are directional couplers (see paragraph [0022], lines 3-8 and FIG.6a where in the light comes from the fiber link 51 are directly coupled into the optical receiver via line pipe or lenses 54 (directional coupler)).

**Regarding to claim 7**, Levy et al. disclose everything claimed as applied above (see claim 6). In addition, Levy et al. disclose the apparatus further includes: wherein the directional couplers include a waveguide or an optical fiber (see paragraph [0022], lines 3-8 and FIG.6a where in the directional coupler 54 is coupled with optical fiber 51).

**Regarding to claims 8 and 9**, Levy et al. disclose everything claimed as applied above (see claim 1). In addition, Levy et al. disclose the apparatus further includes: the couplers are free space couplers wherein the free space couplers are beam splitters (see FIG.6a where in the optical couplers 63 acts as free space coupler and it has a function of beam splitter).

**Regarding to claim 10**, Levy et al. disclose an article of manufacture, comprising a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the operations (see FIG.8) comprising:

converting a signal to communicate with memory devices from a first electrical signal to an optical signal 9 (see paragraph [0035], lines 1-5 and FIG.8 where in the

Art Unit: 2613

OT&R converts the electrical signal from the memory controller to optical signal link 82 for communicating with DIMMs 30 which has memory device 12);

propagating the optical signal on an optical bus (optical bus 82) to N optical couplers (see FIG.5, FIG.6a and FIG.8 where in DIMMs 30 includes light pipe or lenses 54 (optical coupler));

coupling one-Nth of the optical signal from the optical bus to each one of N optical receivers (see paragraph [0035], lines 1-5; FIG.6a and FIG.8 where in one-Nth of the optical signal from the optical bus 82 is coupled into one of the DIMMs 30 which includes optical receiver 61);

each optical receiver converting its one-Nth of the optical signal to a second set of electrical signals; and coupling the second set of electrical signals to one or more memory devices via N memory modules (see paragraph [0018], lines 19-23 and FIG.3, FIG.6a and FIG.8 where in optical receiver 61 converting the optical signal to the second electrical signal using signal converter 35 which is on the substrate 31 inside the DIMMs 30 for usage by the memory device 12) .

**Regarding to claim 11**, Levy et al. disclose everything claimed as applied above (see claim 10). In addition, Levy et al. disclose the apparatus further includes: wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising propagating the optical signal on optical fiber (see paragraph [0028], lines 1-2 and FIG.5).

**Regarding to claim 12**, Levy et al. disclose everything claimed as applied above (see claim 11). In addition, Levy et al. disclose the apparatus further includes: wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising coupling one-Nth of the optical signal from the optical bus to each one of N optical receivers via a directional coupler (see paragraph [0022], lines 3-8 and FIG.6a where in the light comes from the fiber link 51 are directly coupled into the optical receiver via line pipe or lenses 54 (directional coupler).

**Regarding to claim 13**, Levy et al. disclose everything claimed as applied above (see claim 10). In addition, Levy et al. disclose the apparatus further includes: wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising propagating the optical signal via free space (see FIG.5 where in propagating the optical signal along the optical bus 52 and 53 has free space propagation).

**Regarding to claim 14**, Levy et al. disclose everything claimed as applied above (see claim 13). In addition, Levy et al. disclose the apparatus further includes: wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising coupling one-Nth of the optical signal from the optical bus to each one of N optical receivers via a beam splitter (semi-transparent mirrors 63) (see paragraph [0022], lines 3-8 and FIG.6a).

**Regarding to claim 15**, Levy et al. disclose an apparatus comprising:

one or more memory devices (memory device 12) to communicate with an integrated circuit (a substrate), the integrated circuit having an optical receiver (OT&R) (see paragraph [0020], lines 8-11; paragraph [0020], lines 2-4 and FIG.5) ;

N memory modules (DIMMs 30) coupled to the memory devices (memory device 12) (see paragraph [0020], lines 13-16 and FIG.5);

N optical transmitters coupled to the N memory modules (see FIG.5 and FIG.6a where in optical transmitter 62 exists in the optical interface 33 couples to the memory module (DIMMs 30)) ; and

an optical bus coupled to the optical receiver (see FIG.6a where in optical receiver 61 couples to the optical bus 51),

each of the N optical transmitters to convert a signal to communicate with the integrated circuit from an electrical signal to an optical signal (see paragraph [0028], lines 1-6; FIG.5 and FIG.6 where in optical transmitter inside the optical connector housing 33 needs to convert the electrical signal from the memory device 12 to optical signal in order to communicate with the integrated circuit which includes optical transmitting and receiving (OT&R) device through dual optical fibers)

the optical bus to propagate the optical signals to the optical receiver, the optical receiver to convert the optical signals to electrical signals (see paragraph [0018], lines 19-23 and FIG.3, FIG.6a and FIG.8 where in optical receiver 61 converting the optical

signal to the second electrical signal using signal converter 35 which is on the substrate 31 inside the DIMMs 30 for usage by the memory device 12).

**Regarding to claim 16**, Levy et al. disclose everything claimed as applied above (see claim 15). In addition, Levy et al. disclose the apparatus further includes: wherein the integrated circuit is a memory controller (see paragraph [0018], lines 19-23 and FIG.5).

**Regarding to claim 17**, Levy et al. disclose everything claimed as applied above (see claim 15). In addition, Levy et al. disclose the apparatus further includes: wherein the integrated circuit is a processor (see FIG.8 where in the integrated circuit of memory controller and OT&R also couple with microprocessor).

**Regarding to claims 18 and 21**, Levy et al. disclose everything claimed as applied above (see claim 15 and 20). In addition, Levy et al. disclose the apparatus further includes: wherein the optical bus includes optical fiber (see paragraph [0028], lines 1-2 and FIG.5).

**Regarding to claim 19**, Levy et al. disclose everything claimed as applied above (see claim 15). In addition, Levy et al. disclose the apparatus further includes: wherein the optical receiver includes a photodiode (see FIG.5 where in it is well known in the art that a photodetector inherently exists in the optical receiver (OT&R) for converting the input optical signal to electrical signal).

**Regarding to claim 20**, Levy et al. disclose everything claimed as applied above (see claim 15). In addition, Levy et al. disclose the apparatus further includes: wherein the couplers are directional couplers (see paragraph [0022], lines 3-8 and FIG.6a where in the light comes from the fiber link 51 are directly coupled into the optical receiver via line pipe or lenses 54 (directional coupler)).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 22-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy et al. (US Pub Number 2004/0126115) in view of Sheaffer (US Pub Number 2003/0188244).

**Regarding to claim 22**, Levy et al. disclose a system (see FIG.5), comprising:  
an integrated circuit (a substrate) to communicate with a memory (memory device 12), the integrated circuit having an optical transmitter (OT&R) (see paragraph [0020], lines 8-11; paragraph [0020], lines 2-4 and FIG.5) ;

an optical bus (optical connection system 51) coupled to the optical transmitter (see paragraph [0020], lines 4-6 and FIG.5);

N optical receivers (receiver 61) coupled to the optical bus via N optical couplers (light pipe or lenses 54) (see paragraph [0022], lines 1-8; FIG.5 and FIG.6a where in plurality of optical receivers inside the optical connector housings 33 couple to the optical bus through plurality of optical light pipe or lenses inside the optical connector housings 33);

N memory modules (DIMMs 30) coupled to the N optical receivers (see paragraph [0022], lines 17-19; FIG.5 and FIG.6a where in plurality of DIMM 31 couple to the plurality of optical receivers inside the optical connector housings 33); and

one or more memory devices (memory device 12) coupled to the N memory modules (DIMMs 30) (see paragraph [0020], lines 13-16 and FIG.5),

the optical transmitter to convert a signal to communicate with the memory devices from a first electrical signal (an electrical link 46) to an optical signal (see paragraph [0020], lines 2-4; paragraph [0035], lines 2-6 and FIG.5 where in the OT&R converts the electrical signal from the electrical link 46 to optical signal link 52 for communicating with DIMMs 30 which has memory device 12), the optical bus to propagate the optical signal (see paragraph [0020], lines 4-6 and FIG.5 where in optical bus 52 for propagating the optical signal in it), each of the N optical couplers to couple one-Nth of the optical signal from the optical bus to its associated optical receiver (see paragraph [0035], lines 1-5; FIG.6a and FIG.8 where in one-Nth of the optical signal from the optical bus 82 is coupled into one of the DIMMs 30 which includes optical receiver 61),

each optical receiver to convert its one-Nth of the optical signal to second set of electrical signals, the N memory modules to couple the second set of electrical signals to the memory devices (see paragraph [0018], lines 19-23 and FIG.3, FIG.6 and FIG.8 where in optical receiver 61 converting the optical signal to the second electrical signal using signal converter 35 which is on the substrate 31 inside the DIMMs 30 for usage by the memory device 12).

Even though Levy et al. disclose an integrated circuit, which has memory controller, optical transmitter and optical receiver device, communicates with memory device, Levy et al. fails to disclose the graphic controller, which is coupled to the integrated circuit for displaying purpose.

Sheaffer discloses a system, which has graphic controller that is coupled to the memory controller of the integrated circuit chip for controlling the display of information on a suitable display 132 (see paragraph [0026] and FIG.1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Levy et al.'s invention as to use graphic controller for controlling the display of information on a display because it would allow optical communication system with memory device having accurate and useful display system for displaying the receiving data signal.

**Regarding to claim 23**, Levy et al. disclose everything claimed as applied above (see claim 22). In addition, Levy et al. disclose the apparatus further includes: wherein the integrated circuit is a memory controller (see paragraph [0018], lines 19-23 and FIG.5).

**Regarding to claim 24**, Levy et al. disclose everything claimed as applied above (see claim 22). In addition, Levy et al. disclose the apparatus further includes: wherein the integrated circuit is a processor (see FIG.8 where in the integrated circuit of memory controller and OT&R also couple with microprocessor).

**Regarding to claim 25**, Levy et al. disclose an apparatus comprising:  
one or more memory devices (memory device 12) to communicate with an integrated circuit (a substrate), the integrated circuit having an optical receiver (OT&R) (see paragraph [0020], lines 8-11; paragraph [0020], lines 2-4 and FIG.5) ;

N memory modules (DIMMs 30) coupled to the memory devices (memory device 12) (see paragraph [0020], lines 13-16 and FIG.5);

N optical transmitters coupled to the N memory modules (see FIG.5 and FIG.6a where in optical transmitter 62 exists in the optical interface 33 couples to the memory module (DIMMs 30)) ; and

an optical bus coupled to the optical receiver (see FIG.6a where in optical receiver 61 couples to the optical bus 51),

each of the N optical transmitters to convert a signal to communicate with the integrated circuit from an electrical signal to an optical signal (see paragraph [0028], lines 1-6; FIG.5 and FIG.6 where in optical transmitter inside the optical connector housing 33 needs to convert the electrical signal from the memory device 12 to optical signal in order to communicate with the integrated circuit which includes optical transmitting and receiving (OT&R) device through dual optical fibers)

the optical bus to propagate the optical signals to the optical receiver, the optical receiver to convert the optical signals to electrical signals (see paragraph [0018], lines 19-23 and FIG.3, FIG.6a and FIG.8 where in optical receiver 61 converting the optical signal to the second electrical signal using signal converter 35 which is on the substrate 31 inside the DIMMs 30 for usage by the memory device 12).

Even though Levy et al. disclose an integrated circuit, which has memory controller, optical transmitter and optical receiver device, communicates with memory device, Levy et al. fails to disclose the graphic controller, which is coupled to the integrated circuit for displaying purpose.

Sheaffer discloses a system, which has graphic controller that is coupled to the memory controller of the integrated circuit chip for controlling the display of information on a suitable display 132 (see paragraph [0026] and FIG.1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Levy et al.'s invention as to use graphic controller for controlling the display of information on a display because it would allow optical communication system with memory device having accurate and useful display system for displaying the receiving data signal.

**Regarding to claim 26**, Levy et al. disclose everything claimed as applied above (see claim 25). In addition, Levy et al. disclose the apparatus further includes: wherein the integrated circuit is a memory controller (see paragraph [0018], lines 19-23 and FIG.5).

**Regarding to claim 27**, Levy et al. disclose everything claimed as applied above (see claim 25). In addition, Levy et al. disclose the apparatus further includes: wherein the integrated circuit is a processor (see FIG.8 where in the integrated circuit of memory controller and OT&R also couple with microprocessor).

#### ***Citation of Pertinent Prior Art***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Baker et al. (US Pub Number 2003/0043426) disclose optical interconnect in high-speed memory system having optical transceiver with optical bus.

Gordon et al. (US Pub Number 2003/0202748) disclose tri-state optical system and method having optical transceiver with optical bus.

Art Unit: 2613

**Conclusion**

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHYOWAI LIN whose telephone number is (571) 270-1659. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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KENNETH VANDERPUYE  
SUPERVISORY PATENT EXAMINER

Application/Control Number: 10/748,758

Art Unit: 2613

Page 17